

I am pleased to welcome this book to the cannon of VMM literature. I hope you will find it helpful in appreciating the power of the VMM methodology and ease your adoption of it.
Janick Bergeron, Synopsys Scientist

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... "A Pragmatic Approach to Adopting VMM..." is exactly what the doctor ordered for demystifying the VMM methodology and focusing users on the keys to applying it efficiently.
Scott Sandler, President and CEO



... teaches by example how the constructs in SystemVerilog are used to implement the methodology presented in the VMM. Similar to learning from an experienced mechanic how to use the right tools to repair a car, this book provides a way to learn from experts the right way to use SystemVerilog for verification, and makes it is much easier to understand how to apply the VMM methodology on actual designs.
Stuart Sutherland, SystemVerilog instructor, President of Sutherland HDL, Inc.

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... can be seen as a long overdue training on best practices for writing System-Verilog-based testbenches. Companies should adopt this approach, if only to save cost, as verification engineers have better things to do than redevelop and learn a new testbench environment every time they change projects.
Alain Raynaud, Technical Director, EVE USA, inc.



... helps the reader to quickly get on board in the application of VMM for verification because it demonstrates through complete simulatable examples various approaches in building reusable VMM compliant testbenches. ... uses simple illustrations to explain the concepts involved in building of SystemVerilog based verification environments for complex SOCs.
Vikas Gautam, Director, Corporate Applications Engineering, Verification Group, Synopsys

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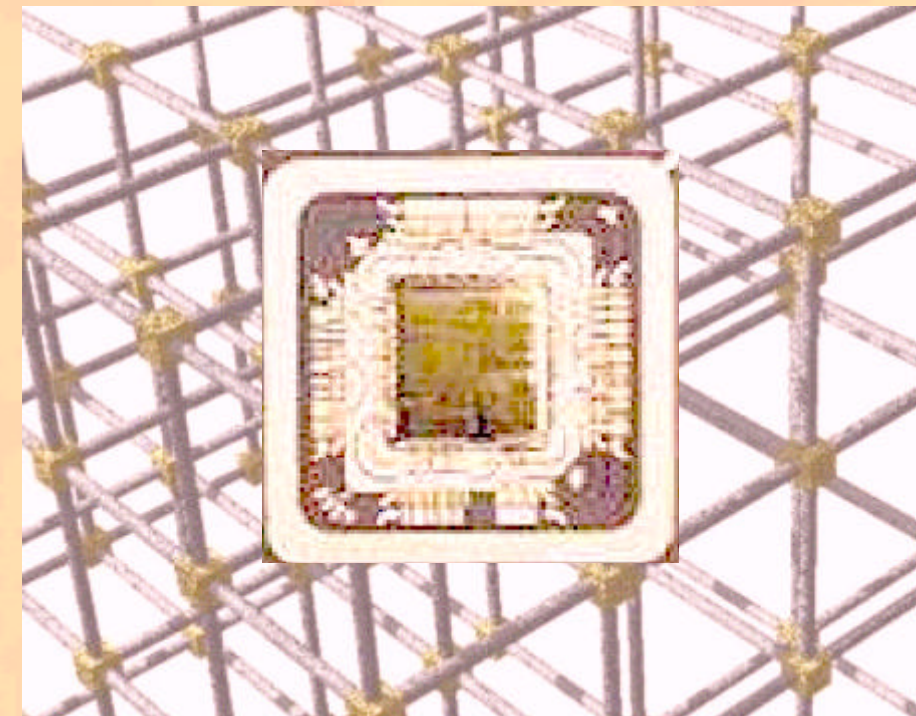


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A Pragmatic Approach to VMM Adoption

A Pragmatic Approach to VMM Adoption

... a SystemVerilog Framework for Testbenches



Ben Cohen
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